IN THE SPECIFICATION

Please amend the paragraphs listed below to read as follows:

[0023] FIG. 2A shows spacer pull-down of spacers 26S extending down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D. FIG. 2A shows the structure of the SOI device 10_2 in accordance with this invention, prior to epitaxial growth of the raised source/drain regions 28S/28D of FIG. 2B on the surface of the thin silicon layer 12 of the device 10. The device 10 includes a thin silicon layer 12 formed on a Buried OXide (BOX) layer 12. A gate electrode stack is formed on the thin silicon layer 12. The gate electrode stack includes a dielectric (gate oxide) layer 14 formed above the thin silicon layer 12; a gate electrode 18 composed of polysilicon above the gate dielectric layer 14; the notched amorphous silicon, cap layer 21 bordered by the dielectric plugs 26P formed on the upper surface the gate electrode 18; and the hard mask 22 covering the upper surfaces of the amorphous silicon, cap layer 21 and the upper surfaces of the dielectric plugs 26P. Sidewall spacers 26S composed of silicon oxide have been formed on the sidewalls of the gate electrode 18 which cover the sidewall surfaces of the gate electrode 18 entirely. ~~and which~~ The sidewall spacers 26S reach up high enough from the silicon layer 12 to overlap the edges of the dielectric plugs 26P. The amorphous silicon cap layer 21 and the dielectric plugs 26P are covered by the hard mask 22. In other words, the sidewall spacers 26S, which cover the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P, which fill the notches 24, as shown in FIGS. 3F and 3G. The dielectric plugs 26P are formed at the top of the gate electrode 18 by etching away the outer edges of amorphous silicon cap layer 21 thereby recessing the periphery of the amorphous silicon cap layer 21 as described below with reference to FIGS. 3H and 3I.

[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D, i.e. [[T]] there is no spurious growth on the top corner of the polysilicon of the gate electrode 18 of the kind seen in FIG. 1B adjacent to the dielectric plugs 26P. The tops of the sidewall spacers 26S, in addition to covering the sidewalls of the gate electrode 18, are contiguous with and overlap the outer edges of the dielectric plugs 26P.

[0025] FIGS. 3A-3J illustrate the process flow employed to construct the structure of FIGS. 2A and 2B. One advantage of [[this]] the method/structure of this invention is that there is very little processing required above the normal process flow. The key is to form a ~~top-notched gate~~ Top Notched Gate (TNG) structure ~~(TNG)~~ with notches 24 shown in FIGS. 3F and 3G, which can then be filled as illustrated by FIGS. 3H and 3I with a set of dielectric plugs 26P during the normal process flow. The structure is formed using the following steps.

[0027] FIG. 3A shows a potential gate electrode stack ~~comprising SOI material~~ formed on a Buried OXide (BOX) layer 11 of silicon dioxide covered with a conventional SOI thin silicon layer 12. [[First]] Then a blanket layer of gate oxide layer 14B was formed on the top surface of BOX layer 11. Next, a blanket polysilicon layer 18B was formed on the top surface of gate oxide layer 14B. The blanket polysilicon layer 18B may be doped or undoped.

[0032] FIG. 3F shows the device 10 of FIG. 3E after the TNG selective formation of the undercut notches 24 in the amorphous silicon cap layer 21B of FIG. 3E. In this step the undercut notches 24 are formed below the outer edges of the hard mask 22 thereby forming a recessed amorphous silicon cap 21 between the notches 24 above the blanket gate electrode layer 18B. Selective undercut of the amorphized layer 21B is done to form the notched amorphous silicon cap 21. The selective undercut is done during polysilicon RIE (described in detail below). In other words, an RIE etching process removes the peripheral portion of the amorphous silicon cap layer 21B to form recesses 24 at the edges thereof producing the notched amorphous silicon cap 21 which remains intact between the notches 24 and below the hard mask 22 which remains intact as shown in FIGS. 3E and 3F.

[0034] FIG. 3H shows the device 10 of FIG. 3G after blanket deposition of a sidewall spacer layer 26B composed of an appropriate sidewall spacer material covering the surface of device 10 while at the same time it is filling the notches 24 on the recessed edges of the amorphous silicon cap layer 21 with material, which at this point in the process is an integral part of the sidewall spacer layer 26B. [[which]] That sidewall spacer material will provide the plugs 26P seen in FIGS. 2A, 2B, 3I, and 3J. The sidewall spacer material forming the sidewall spacer layer 26B comprises any sidewall spacer material such as a dielectric material, e.g. silicon oxide or silicon nitride.